

# A Scalable MOS Field Effect Transistor

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## Field of the Invention

This invention relates to semiconductors and more particularly to self aligned metal oxide semiconductor (MOS) field effect transistors (FET's) having submicron gate lengths with a T-shaped gate.

## Background of the Invention

State-of-the-art metal-oxide-semiconductor field effect transistors require shrinking the gate length below 0.25 $\mu$ m. The standard process for forming the gates is by depositing a polysilicon layer, etching this layer to define the required gate length, and using the polysilicon as a mask for the source/drain shallow implant step. The shallow implant step is followed by forming a nitride sidewall spacer, implanting the deep ohmic region in the source/drain and then forming a metal silicide to the gate and the source/drain implant. The resistance of the gate thus increases as the gate length is reduced, because the gate metal silicide has the same gate length as the polysilicon gate underneath. The gate resistance slows down the devices because of the RC time delay. Alternatively, one can form a metal gate which

is longer than the polysilicon gate by opening a window in an oxide layer and patterning metal. This process has produced the fastest silicon devices to date, but requires a highly critical realignment to the initial polysilicon gate, which if not successful, would result in shorting the gate with the ohmic source/drain contacts. Therefore the above process is not compatible with manufacturing.

In addition to an increase in gate resistance due to scaling down the gate length in MOS FET's, the ohmic source/drain contacts formed by ion implantation cannot be scaled in depth as required to keep the aspect ratio of gate length to junction depth greater than 1. As the <sup>gate length</sup>~~width~~ of the MOS FET's are scaled, <sup>to smaller dimensions</sup>~~the resistance~~ of the ohmic regions increases, which degrades the speed performance of the FETs. The threshold voltage has to be adjusted by a channel implant, which has to become shallower in order to prevent short channel effects. The shallower implant, in turn, reduces the carrier mobility in the inversion layer, and is also becoming more difficult to control.

### Summary of the Invention

In accordance with the present invention, a structure and process sequence is described for building field effect transistors which can easily be scaled to submicron dimensions both in length and in width. The process relies on forming either Schottky metal ohmic source/drain contacts or raised, in-situ doped epitaxial ohmic contacts, and a metal or metal/polysilicon gate which is self aligned and may have a T-shape in order to reduce the parasitic gate resistance.

The invention provides a process for forming the gate stack, which allows a T-shaped metal gate with no critical alignment steps, and which results in a greatly reduced gate resistance.

The invention further provides a process which allows the formation of extremely shallow source/drain contacts, which are scalable in area.

The invention eliminates the need for gate stack silicon nitride sidewall spacers.

The invention further provides a new process that allows the formation of T-gates, self aligned to existing shallow source-drain contacts, without any critical alignment needed for example an alignment accuracy of about 0.2  $\mu\text{m}$  for a gate length in the range

of 0.05 to 0.2 $\mu$ m.

a The invention further provides a new alternative process where the gate is formed by <sup>L.I.</sup><sub>1</sub> metal or metal/polysilicon combination, without any silicidation needed, and results in an extremely low gate contact resistance.

10 The invention further provides a new process in which the source/drain contacts can be made by either a metal barrier or junction or an in-situ-doped semiconductor with respect to the channel, thus avoiding ion implantation and annealing. The high conductivity of the contacts described herein allows the scaling of the area of the contacts for high packing density circuits.

The invention further provides a self aligned raised epitaxial channel formed between raised semiconductor regions forming the source and drain.

15 The invention further provides a new process in which the same source/drain contact metal, for example titanium, can be selectively and locally oxidized to form the gate dielectric material, titanium dioxide, having a high dielectric constant, thus relaxing the scaling limits on the gate dielectric thickness.

### Brief description of the Drawing

These and other features, objects, and advantages of the present invention will become apparent upon a consideration of the following detailed description of the invention when read in conjunction with the drawings, in which:

Fig. 1 is a cross section view illustrating early steps in forming the embodiment shown in Fig. 7.

Fig. 2 is a top view of the structure of Fig. 1 after the step of etching.

Fig. 3 is a cross section view along the line 3-3 of Fig. 2.

Figs. 4-6 are cross section views illustrating further steps in forming the embodiment shown in Fig. 7.

Fig. 7 is a cross section view of one embodiment of the invention.

Fig. 8 is a graph of the Drain-Source Current verses Drain-Source Voltage showing measurements made for the embodiment shown in Fig. 7.

Figs. 9-11 are cross section views illustrating the fabrication steps in forming the embodiment shown in Fig. 12.

Fig. 12 is a cross section view of a second embodiment of the invention.

Figs. 13-15 are cross section views illustrating the fabrication steps in forming the embodiment shown in Fig. 16.

5 Fig. 16 is a cross section view of a third embodiment of the invention.

Fig. 17 is a cross section view of a fourth embodiment of the invention.

10 Figs. 18 and 19 are cross section views illustrating process steps using ion implantation and for protecting the channel during ion implantation in forming the embodiment shown in Fig. 20.

Fig. 20 is a cross section view of a fifth embodiment of the invention.

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## Description of the Preferred Embodiments

Referring now to the drawing, Fig. 1 shows a cross section view of substrate 12, a sacrificial layer 14, a metal layer 16 which subsequently forms a Schottky barrier or junction with respect to the channel, and an insulating layer 18. Substrate 12 may be a single crystal semiconductor material suitable to form the channel of a MOS FET to be built. Substrate 12 may be, for example, silicon, silicon germanium, germanium, gallium arsenide, indium gallium arsenide, indium phosphide, and indium gallium arsenide phosphide. Sacrificial layer 14 is of a material which may be selectively etched with respect to substrate 12 and which may be consumed by Schottky metal layer 16, for example, in the form of a silicide or germanide. Sacrificial layer 14 functions to protect the channel from reactive ion etching (RIE) damage. Sacrificial layer 14 may be for example silicon germanium with a germanium content  $x$  where  $x$  is equal to or greater than 0.3 and the silicon content is  $1-x$ . Sacrificial layer 14 may also be GaAs, InGaAs, InP,  $\text{In}_{1-x}\text{Ga}_x\text{As}_y\text{P}_{1-y}$  and Si. The material for metal layer 16 forms the source and drain of the MOS FET and is of a material having an appropriately selected work function. Metal layer 16 may be, for example, Co, Ni, Pd, Pt, Rh, Ta, Ti, W, combinations thereof and alloys thereof to provide a selected barrier height and may be blanket deposited by evaporation or sputtering. Metal layer 16 is then covered by insulating layer 18 which may be for example

a low temperature deposited oxide such as by CVD using tetra ortho ethyl silicate (TEOS) as the precursor.

5 Next, a resist is deposited on insulating layer 18 and lithographically patterned to define a gate window 19 and future source and drain regions as shown in Fig. 2. The gate window is opened through insulating layer 18 and metal layer 16 by using for example RIE. A trench is formed around future source and drain regions. Fig. 3 shows a cross section view along the line 3-3 of Fig. 2. Fig. 3 shows a sacrificial layer 14 over substrate 12 in gate window 19 such that the RIE damage does not reach the channel of the MOS FET to be built.

10 Next as shown in Fig. 4, metal layer 16 and sacrificial layer 14 underneath it are alloyed to form source and drain contacts 20 and 22 while not disturbing sacrificial layer 14 in gate window 19. Source and drain contacts 20 and 22 form Schottky barriers or junctions 23 and 24, respectively, with channel 25 in substrate 12 shown in Fig. <sup>5</sup>~~4~~. The ratio of thickness of metal layer 16 to sacrificial layer 14 and the temperature are adjusted to permit complete alloying of layer 14 to form Schottky source and drain junctions to the channel. There may be some alloying with substrate 12 at the original substrate 12 interface. The penetration of alloying into substrate 12 is slight and just enough to remove the heterojunction of <sup>sacrificial</sup>~~sacrificial~~ layer 14 and substrate 12. For example, sacrificial layer 14 may be SiGe, substrate 12



may be Si, and Schottky metal layer 16 may be Ti for a n channel FET. Upon the step of siliciding which may occur at a temperature at or above 600°C, a silicide or mixed silicide may be formed, for example, titanium silicide and titanium germanide. For a p channel FET, Schottky metal layer 16 may be for example Pt. Upon the step of siliciding at or above 250°C, platinum silicide and platinum germanide may be formed.

Next as shown in Fig. 5, a gate <sup>dielectric</sup>~~oxide~~ 26 is formed or grown on substrate 12 in gate window 19, sidewalls 27 and 28 of gate window 19 and the upper surface of insulating layer 18. ~~Gate oxide 26 may~~ have a thickness in the range from 2 to 20 <sup>nm</sup> and typically 3 to 5 nm. <sup>Insert 2</sup>

Referring to Fig. 6, a gate material 30 which may be, for example, Al, W, with or without appropriate diffusion barriers and with or without polysilicon underneath is either blanket deposited or grown over gate <sup>dielectric</sup>~~oxide~~ 26 and patterned lithographically to define a T-shaped gate 32. T-shaped gate 32 extends over ~~insulating sacrificial layer 14~~ <sup>18</sup> above gate <sup>dielectric</sup>~~oxide~~ 26. A negative resist may be used in the process of patterning lithographically.

An insulating material 34 which may be, for example, silicon dioxide or a flowable oxide is formed over exposed gate <sup>dielectric</sup>~~oxide~~ 26 and T-shaped gate 32. Holes or openings 35 may be opened through insulating material 34 as shown in Fig. 7. The holes or openings 35 may be subsequently filled with conductive material 36 for

b example tungsten and planarized via chemical mechanical polish (CMP) to form vias <sup>coplanar</sup> ~~co-planar~~ with the upper surface of insulating material 34 (not shown). Alternatively, a metal layer 37 may be formed filling holes 35 with conductive material 36 and forming a layer on insulating material 34. Metal layer 37 may be patterned to provide circuit interconnections.

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Fig. 8 shows a graph of the drain-source current versus drain source voltage for the embodiment of Fig. 7 with a gate length of  $0.25\mu\text{m}$ . The FET measured was an n channel with source contact 20 and drain contact 22 being a mixture of titanium silicide and titanium germanide formed by alloying a titanium layer 16 with a sacrificial layer of  $\text{SiGe}_x$  where  $x$  is .3. The metal gate had a layer of Ti of 50 Angstroms and a layer of Al of 1500 Angstroms. The top or T length of the T shaped gate was  $0.5\mu\text{m}$ . In Fig. 8 the ordinate represents drain-source current and the abscissa represents drain-source voltage. Curves 44-47 were plotted from measurements with the gate voltage at 0.5V, 1.0V, 1.5V and 2.0V respectively. The transconductance  $g_m$  was equal to about 210 mS/mm and output conductance  $g_d$  was equal to about 10 mS/mm.

20 Referring to Fig. 9, a cross section view is shown of the early steps of a process for forming the embodiment shown in Fig. 12. In Figs. 9-12, like references are used for functions corresponding to the apparatus of Figs. 1-7.

Referring again to Fig. 9, a semiconductor layer 40 is formed on substrate 12. Semiconductor layer 40 may be a single crystal or a polycrystalline material which can be selectively etched by way of a wet etch or RIE with respect to substrate 12. For example, substrate 12 may be silicon and semiconductor layer 40 may be silicon germanium alloy or vice versa or, substrate 12 may be GaAs and semiconductor layer 40 may be InGaAs or vice versa. Semiconductor layer 40 may be highly doped, for example, in the range from  $5 \times 10^{19}$  to  $5 \times 10^{20}$  atoms/cm<sup>3</sup> and functions as the source and drain of the MOS FET shown in Fig. 12. Semiconductor layer 40 may be doped p-type for a p channel MOS FET and doped n-type for an n channel MOS FET. Semiconductor layer 40 may be epitaxially formed in-situ over substrate 12. Semiconductor layer 40 may then be covered by insulating layer 18 which may be for example an oxide formed at low temperature. Referring to Fig. 10, lithography is then used to open gate window 19 in insulating layer 18 and semiconductor layer 40 using for example, RIE.

Referring to Fig. 11, a gate ~~oxide~~<sup>dielectric</sup> 26 is deposited in gate window 19 on substrate 12 and over the upper surface of insulating layer 18.

Referring to Fig. 12, a gate material 30 is formed over gate ~~oxide~~<sup>dielectric</sup> 26 and patterned lithographically to define a T-shaped gate 32. Gate material 30 extends from gate window 19 over the upper surface of insulating layer 18 with or without gate oxide

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b therebetween. Gate <sup>dielectric</sup> ~~oxide~~ 26 may be removed over insulating layer 18 prior to depositing gate material 30.

Fig. 13 shows the early steps in forming an MOS FET shown in Fig 16. In Figs. 13-16 like references are used for functions corresponding to the apparatus of Figs. 1-7 and 9-12. Substrate 12 has on its upper surface metal layer 16 which may be any metal, for example, <sup>Al, Er, Hf, Nb, Pt, Ta, Ti, Y, W, or Zr</sup> ~~titanium or platinum~~. An insulating layer 18 which may be for example silicon nitride is formed on the upper surface of Schottky metal layer 16.

10 A gate window 19 is formed in insulating layer 18 as shown in Fig. 14. After opening gate window 19, metal layer 16 where exposed is oxidized to form for example  $TiO_2$  which becomes gate dielectric 50 as shown in Fig. 15. If the temperature is kept below  $700^\circ C$  during oxidation then substrate 12 if silicon will not oxidize at the interface.

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Next, a gate material 30 is formed over gate dielectric 50 and patterned lithographically to define a T-shaped gate 32 as shown in Fig. 16.

20 In a variation shown in Fig. 17, after opening the gate window 19 in the Schottky metal layer 16 shown in Fig. 3 or in in-situ heavily doped layer 40 shown in Fig. 10, the sample or substrate 12 may be inserted in an epitaxial growth system, which can

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5 selectively grow a required semiconductor such as Si or SiGe in gate opening 19 on substrate 12 to form channel 52 without growing a semiconductor on top of insulating layer 18 of silicon dioxide or silicon nitride ~~or on gate dielectric 26~~. The epitaxial layer forming channel 52 results in a raised FET channel which is in electrical or actual contact from both sides by the source 41 and drain 42. Lattice strain can be introduced in channel 52 by growing a heterostructure such as Si/SiGe and/or graded compositions in order to make use of enhanced transport properties (e.g. mobility) as described in US Patent 5534713 which issued on July 9, 1996 to K. E. Ismail, a coinventor herein and F. Stern which is assigned (one half) to the assignee herein and which is incorporated herein by reference to show the formation of strained layers to increase mobility etc.

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In Figs. 17-20, like references are used for functions corresponding to the apparatus of Figs. 1-7 and 9-16.

20 In another variation as shown in Figs. 18-20, an insulating layer 18 is first deposited on substrate 12 and then lithographically patterned to open or form gate window 19 in insulating layer 18 which may be for example silicon dioxide. Gate window 19 can be filled by metal for example Ti using resist lift off or by a semiconductor such as Ge using selective growth. In both cases the gate window is filled with material that is chosen such that it can stop the implanted species during implant of the

source and drain which are implanted through insulating layer 18 for forming shallow self aligned source region 54 and drain region 56. The window material which may be for example Ge as shown in Fig. 18 or Ti as shown in Fig. 19 can thus easily be selectively etched with respect to the semiconductor substrate 12 underneath, substrate 12 which may be for example Si or SiGe alloy or combinations thereof. Following an annealing step to activate the implant, gate <sup>dielectric</sup>~~oxide~~ 26 is deposited and the rest of the process for forming the T-gate for the FET is done.

In all of the above proposed processes, the choice of the ohmic contacts and the gate metal, depends on the required threshold voltages and the device design. The work function of the metal used for source and drain contacts as shown, for example in Figs. 7 and 16, is a subject of optimization. The higher the Schottky barrier height between the metal and the semiconductor, the higher the series access resistance from source and drain contacts to the channel. On the other hand, electrons or holes overcoming this barrier have to be very energetic and hence have a high injection velocity and maintain this velocity under the gate. Highly-doped semiconductor source and drain contacts as shown in Fig. 12 have lower injection barriers but are also more resistive than metal contacts. Therefore, depending on the application and the threshold voltages required, one or the other processes shown above can be chosen to build corresponding FET's shown in Figs. 7,

12 and 16.

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The invention described herein can be used in building field-effect transistors such as metal-semiconductor FET's, modulation-doped FET's, metal-oxide-semiconductor FET's and circuits. Compared to existing process steps of such FET's, the structure and process of this invention can result in a greatly reduced gate resistance, and extremely shallow ohmic contacts. The combination of the above two effects results in higher FET device and circuit speeds. The advantage of using a Schottky metal for example titanium or platinum for the source and drain which is self aligned to the channel of the FET, allows very high injection velocity of carriers into the channel, and also scaling down the transistor width and area, since the metal remains highly conducting until the size approaches the size of the grains, which may be more than three orders of magnitude smaller than the area used for the source and drain in state-of-the-art FET devices.

While there has been described and illustrated an FET structure and method of making self aligned Schottky metal silicide and/or germanide source and drain contacts and a T-shaped gate or a heavily doped semiconductor material as the source and drain with a T-shaped gate, it will be apparent to those skilled in the art that modifications and variations are possible without deviating from the broad scope of the invention which shall be limited solely by the scope of the claims appended hereto.